REMARKS

Status of the Claims

Prior to entry of this amendment, claims 1-26 are pending in the application. All pending claims stand rejected as follows:

- Claims 1-6, 11-15, 18-20, and 22-23 are rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by U.S. Publication No. 2001/0026997 A1 to Henley *et al.* ("Henley").
- Claims 7-10, 16-17, 21, and 24-26 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Henley in view of U.S. Patent No. 4,764,248 to Bhattacherjee *et al.* ("Bhattacherjee").

Claim Amendments and Interview Summary

Applicants thank Examiner Brewster for his time and courtesy extended during a telephonic interview with the undersigned attorney on October 18, 2005. The following is intended to constitute a proper recordation of the interview in accordance with M.P.E.P. §713.04, and also to provide a full response to the Office Action.

The discussion during the interview focused on independent claim 1, as well as on differences between the present invention and Henley. Consistent with this discussion, Applicants have amended claim 1. In addition, Applicants added new claims 51-66. No new matter has been introduced by these claims changes. Support for the amendment to claim 1 can be found throughout the specification, for example, in paragraphs **[0004]**, **[0010]**, and **[0058]**. Also, support for the new claims can be found in claims 1-26, as originally filed.

Upon entry of this amendment, claims 1-26 and 51-66 will be pending and under consideration. In view of the above amendments and following remarks, reconsideration and withdrawal of all grounds of rejection are respectfully requested.

Rejections under 35 U.S.C. §102(e)

Claims 1-6, 11-15, 18, 20, and 22-23 are rejected under 35 U.S.C. §102(e) as allegedly being anticipated by Henley. Applicants respectfully traverse this rejection at least because Henley does not teach a method of forming a semiconductor structure that includes "*processing*

the semiconductor structure to form a CMOS device at least partially thereover, the CMOS device having a channel through the strained semiconductor layer," as recited in independent claim 1, as amended.

As explained in the Applicants' specification, thin, near-surface, strained heteroepitaxial layers constitute critical parts of devices formed on virtual substrates, and it is desirable to avoid the consumption of these layers during CMOS processing. To that end, in various embodiments, the claimed invention contemplates depositing a screening layer to impede consumption of the surface material in heterostructure-based wafers, such that sufficient thickness of that material is available for device channels. See Specification, paragraphs **[0004]**, **[0010]-[0012]** and **[0058].**

In contrast, Henley discloses a method for fabricating a silicon-on-insulator substrate via a controlled cleaving action. In Henley, a compressive SiGe layer (103, 203) is formed over a bulk Si substrate, and then a Si device layer (105) is epitaxially formed over the compressive layer. Then, a controlled cleaving action is initiated and maintained at the compressive layer to free the material layer (105) from the bulk substrate using a propagating cleave front. Preferably, the bulk substrate structure is bonded to a handle wafer prior to cleaving, such that the device layer overlies the handle wafer. See Henley, paragraphs **[0002]** and **[0010].** Applicants respectfully submit that Henley does not teach a method of forming a semiconductor structure that includes "*processing the semiconductor structure to form a CMOS device at least partially thereover, the CMOS device having a channel through the strained semiconductor layer*," as recited in independent claim 1, as amended. Rather, the compressive layer (203) is removed from the device layer (105) and is not used in further device fabrication.

Accordingly, at least for this reason, Applicants respectfully submit that independent claim 1, as amended, is patentable. Without acquiescing to the rejection of claims 2-6, 11-15, 18-20, and 22-23, Applicants note that these claims depend directly from claim 1, as amended, and include all the limitations thereof, and thus, are also patentable. Reconsideration and withdrawal of the rejection of claims 1-6, 11-15, 18, 20, and 22-23 under 35 U.S.C. §102(e) is respectfully requested.

Rejections under 35 U.S.C. §103(a)

Dependent claims 7-10, 16-17, 21, and 24-26 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Henley in view of Bhattacherjee. Without acquiescing to the rejections, Applicants note that these claims depend directly or indirectly from independent claim 1 and include all the limitations thereof. Therefore, Applicants submit that these claims are patentable for at least the reasons independent claim 1, as amended, is patentable.

In addition, with respect to claims 21 and 26, the Office action states on pages 6-7, that it would have been obvious to one of ordinary skill in the art to optimize the thickness of the layers to arrive at the invention claimed in these dependent claims. Applicants respectfully disagree.

As discussed above, Henley discloses a method for removing a thin film of material from a substrate by implanting particles into a stressed layer, thereby reducing a fracture energy level of the substrate. See Henley, paragraphs [0018], [0028], and [0031]. Bhattacherjee discloses a process for minimizing bird's beak in local oxidation of silicon by nitridizing a pad oxide using rapid thermal nitrizidation. See Bhattacherjee, Abstract. Thus, the prior art of record and the claimed invention are aimed at resolving different problems.

In contrast to Henley and Bhattacherjee, various embodiments of the Applicants' invention relate to methods for forming semiconductor structures that include providing one or more layers that impede undesirable consumption of the strained surface material, affect the introduction of dopants by scattering them during implantation, thereby reducing the probability of ion channeling, hinder out-diffusion of dopants during the annealing step, and/or protect the structures against contamination by particles during ion implantation. The thickness ranges of the layers recited in claims 21 and 26 are tailored to obtain the desirable performance of these layers. See Specification at paragraphs [0050] and [0052]. Henley and Bhattacherjee, however, are utterly silent with respect to utilizing screening layers for any of these purposes. Thus, one of skill in the art would find no motivation in Henley and Bhattacherjee, alone or in combination, to provide one or more layers having thickness(es) recited in claims 21 and 26.

In light of the foregoing, reconsideration and withdrawal of the rejection under 35 U.S.C. §103(a) are respectfully requested.

New Claims 51-65

Applicants note that newly-added independent claim 51 is equivalent in scope to claim 1, as examined in the final Office action, that includes all limitations of original dependent claims 19 and 22. Applicants respectfully submit that Henley fails to anticipate this independent claim and all claims dependent therefrom, because Henley does not teach or suggest a *method step* of depositing a screening layer that includes an oxide, recited in claim 51. Instead, Henley discloses depositing a material (i.e. Si) layer over a strained layer and subsequently oxidizing the surface of the material layer to incorporate an oxide layer therein. See Henley, paragraphs [0027] and [0028].

Applicants, therefore, submit that for at least this reason, new claim 51, and claims dependent therefrom, are patentable.

CONCLUSION

Applicants respectfully submit that claims 1-26 and 51-66 are in condition for allowance, and request that application proceed to issue. If, in the Examiner's opinion, a telephonic interview would expedite the favorable prosecution of the present application, the undersigned attorney would welcome the opportunity to discuss any outstanding issues and to work with the Examiner toward placing the application in condition for allowance.

Respectfully submitted,

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